

REMARKS

The Office Action mailed November 19, 2002, has been received and reviewed. Claims 1-7, 9-16 and 18-20 are currently pending in the application. Claims 1-7, 9-16 and 18-20 stand rejected. Applicant has amended claims 1-5, 13-16 and 20, and respectfully request reconsideration of the application as amended herein.

In the "Detailed Action" item 1 of the Official Action of November 19, 2001, the Official Action states

that the instant application does not explicitly describe "the north bridge" in any specific definition or description, thus it is considered for art rejection purpose, the claimed "north bridge chip" is interpreted as a "logic chip" that has the equivalent function as the described core logic unit on page 5, lines 12-13 (Office Action p. 2.)

Applicants respectfully state that a term is entitled to its "plain meaning" definition in the art as well as all other associated definitions included within the present application.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So.

Claims 1-5, 7, 10, 12 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1-5, 7, 10, 12 and 20 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding amended independent claim 1, Applicants claim:

An apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising:
a video input port, for receiving video data for a current video frame;
a video input buffer coupled to the video input port, for storing video data from the video input port;
a previous frame buffer, for storing at least a portion of a previous video frame;
an operation unit coupled to the video input buffer and the previous frame buffer, for **computing a difference frame** from data from the video input buffer and data from the previous frame buffer; and
a result buffer coupled to the operation unit, for temporarily **buffering the difference frame prior to storing the difference frame in the system memory, the apparatus configured to operate within a north bridge chip** of the computer system to enable **the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit.** (*Emphasis added.*)

Regarding claim 1, Dea and So do not appear to teach or suggest an apparatus configured for “computing a difference frame . . . inside of a north bridge chip . . .;” an apparatus configured for “**storing the difference frame in the system memory . . .;**” and an apparatus configured “to enable the **central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit**”, as claimed by Applicants.

Generally, Dea teaches of a “remote video processing system 100 including compression/decompression accelerator 120”, (col. 4, lines 17-20), [wherein] “compression/decompression

accelerator system 120 . . . ha[s] a straight pipeline architecture **rather than shared resources**" (col. 5, lines 24-29). More specifically, accelerator 120, as detailed in FIG. 2, includes:

1. a "frame difference block 220 [wherein] the information of reference frame line 209 [the "previous frame"] **is subtracted from** the current frame information on current frame line 205." (Col. 6, lines 37-40).
2. "A forward discrete cosine transform **is then performed on the data** from frame difference block 220 in encode dataflow 300 by forward discrete cosine transform block 230a." (Col. 10, lines 56-59; emphasis added).
3. "The transformed data from forward discrete cosine transform block 230a **is received by** quantization block 238 . . . **and quantized** therein. The quantized data from block 238 **is applied** by way of quantization output line 216 **to run length encoder** 246 for run length encoding . . . [which] **are applied . . . to encode output circular buffer** 332 (see FIG. 3A) [with] [t]he data within encode output circular buffer 332 [] **then applied to variable length encoder** 112b to provide **compressed bit stream** 338 [while] buffer 332 **may be located in memory** 114 [the "system memory", see FIG. 1]." (Col. 10, line 65 through col. 11, line 11).

Clearly in Dea, the accelerator 120 includes substantial complexity as the difference frame undergoes significant compression processing within accelerator 120 before it is ever stored in the system memory. In fact, Dea teaches away from storing the data in the system memory by disclosing that "accelerator 120 of [Dea's] present invention within remote video interface system 100 ha[s] a straight pipeline architecture **rather than shared resources**." (See col. 5, lines 25-27; emphasis added.) Applicants claim, in amended independent claim 1, an apparatus configured for "computing a difference frame . . . inside of a north bridge chip . . .," an apparatus configured for "storing the difference frame in the system memory . . .," and an apparatus configured "to enable the central processing unit to retrieve the difference frame

directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit”.

Regarding the So reference, the Office Action cites So because it “discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator is provide either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43.” (See Office Action p. 4). Generally, So incorporates digital signal processors (DSPs) at one or more of the bridges, such as at the North bridge and/or South bridge so that the compression and decompression may occur inside of the DSPs of the bridges. So engages in additional compression/decompression complexity within the North bridge and does not disclose an apparatus configured for “computing a difference frame . . . inside of a north bridge chip . . .,” and an apparatus configured for “storing the difference frame in the system memory . . .,” and an apparatus configured “to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit”, as claimed by Applicants in amended independent claim 1. Therefore, Applicants respectfully request that the rejection to claim 1, be withdrawn.

Regarding claims 2-5, 7, 10 and 12, each of these claims includes additional elements that further distinguish from the cited references. In addition to claims 2-5, 7, 10 and 12 depending either directly or indirectly from amended independent claim 1, each of these claims, as a whole, distinguish over the cited references. Therefore, Applicants respectfully request that the rejections to claims 2-5, 7, 10 and 12 be withdrawn.

Regarding claim 20, the Office Action alleges that “claim 20 recites the same limitation as in claim 1 . . .” (Office Action p. 7.) Applicants submit that claim 20 is an independent claim and includes its own elements. Claim 20 recites

A computer system including resources for compressing video, comprising:
 a central processing unit and system memory for further compressing the video within the computer system;
 a video input port, for receiving video data for a current video frame;
 a video input buffer coupled to the video input port, for storing video data

from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an operation unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from data from the video input buffer and data from the previous frame buffer; and

a result buffer coupled to the operation unit, for temporarily buffering the difference frame prior to **storing the difference frame in the system memory**, the video input port, the video input buffer, the previous frame buffer, the operation unit, and the result buffer configured to operate within a north bridge chip of the computer system **to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit.**

② Regarding claim 20, Dea and So do not appear to teach or suggest a computer system configured for "computing a difference frame . . . inside of a north bridge chip . . .," a computer system configured for "**storing the difference frame in the system memory . . .**," and a computer system configured "to enable the **central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit**", as claimed by Applicants. See the arguments above with reference to claim 1.

Clearly in Dea, the accelerator 120 includes substantial complexity as the difference frame undergoes significant compression processing within accelerator 120 before it is ever stored in the system memory. In fact, Dea teaches away from storing the data in the system memory by disclosing that "accelerator 120 of [Dea's] present invention within remote video interface system 100 ha[s] a straight pipeline architecture **rather than shared resources.**" (See col. 5, lines 25-27; emphasis added.) Applicants claim, in amended independent claim 20, a computer system configured for "computing a difference frame . . . inside of a north bridge chip . . .," a computer system configured for "**storing the difference frame in the system memory . . .**," and a computer system configured "to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit".

Regarding the So reference, the Office Action cites So, in claim 1 as now applied to claim 20, because it discloses "the claimed video input buffer being a register that "discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator is provide either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43." (See Office Action p. 4). Generally, So incorporates digital signal processors (DSPs) at one or more of the bridges, such as at the North bridge and/or South bridge so that the compression and decompression may occur inside of the DSPs of the bridges. So engages in additional compression/decompression complexity within the North bridge and does not disclose a computer system configured for "computing a difference frame . . . inside of a north bridge chip . . .;" and a computer system configured for "storing the difference frame in the system memory . . .;" and a computer system configured "to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit", as claimed by Applicants in amended independent claim 20. Therefore, Applicants respectfully request that the rejection to claim 20, be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and further in View of U.S. Patent No. 4,546,383 to Abramatic.

Claims 6 and 13-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Abramatic (U.S. Patent No. 4, 546, 383). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.**

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 6 and 13-16 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 6, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claim 6. Applicants sustain the arguments above that nothing within the four-corners of the cited references teach each and every element of Applicants' invention as claimed, including the elements of the base claim from which claim 6 depends. Namely, Dea, So, and Abramatic do not teach, suggest, or motivate an apparatus configured for "computing a difference frame in the core logic chip . . . ;" an apparatus configured for "storing the difference frame in the system memory . . . ;" and an apparatus configured "to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit" as claimed in Applicants' claim 6. Therefore, Applicants respectfully request that the rejection to claim 6 be withdrawn.

Regarding claims 13-16, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claims 13-16.

Applicants sustain the arguments above that nothing within the cited references teach each and every element of Applicants' invention as claimed in amended independent claim 13 and claims 14-16 depending therefrom. Specifically, Dea, So, and Abramatic do not teach, suggest, or motivate an apparatus configured for "computing a difference frame . . . temporarily buffering the difference frame prior to storing the difference frame in the system memory" and "the apparatus configured to operate within a north bridge chip of the computer system **to enable the central processing unit to retrieve the difference frame directly from the system**

memory via the north bridge chip for further compression of the video data by the central processing unit” as claimed in Applicants’ amended independent claim 13. Therefore, Applicants respectfully request that the rejections to claim 13 and claims 14-16 depending therefrom be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and Further in View of U.S. Patent No. 5,438,374 to Yan.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Yan (U.S. Patent No. 5, 438,374). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 9 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 9, Dea, So, and Yan, either individually, or in any proper combination, do not teach, suggest, or motive Applicants’ invention as claimed in claim 9, including all of the claim limitations of the base claim, namely, an apparatus configured for “computing a difference frame . . . inside of a north bridge chip . . .,” an apparatus configured for “**storing the difference frame in the system memory . . .**,” and an apparatus configured “to enable the central

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processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit”, as claimed by Applicants. In support, Applicants sustain the arguments above as applied to the base claim, amended independent claim 1. Therefore, since Dea, So, or Yan, either individually or in any proper combination, do not teach, suggest, or motivate Applicants’ invention as claimed in claim 9, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 9 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and Further in View of U.S. Patent No. 5,926,223 to Hardiman.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Hardiman (U.S. Patent No. 5, 926, 223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 11 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 11, Dea, So, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants’ invention as claimed in claim 11,

including all of the claim limitations of the base claim, namely, an apparatus configured for "computing a difference frame . . . inside of a north bridge chip . . .," an apparatus configured for "storing the difference frame in the system memory . . .," and an apparatus configured "to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit", as claimed by Applicants. In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in claim 11, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 11 be withdrawn.

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Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So, in View of U.S. Patent No. 4,546,383 to Abramatic and further in view of U.S. Patent No. 5,438,374 to Yan.

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) in view of Abramatic (U.S. Patent No. 4,546,383) and further in view of Yan (U.S. Patent No. 5, 438, 374). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 18 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 18, Dea, So, Abramatic, and Yan, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claim in claim 18, including all of the claim limitations of the base claim, namely, an apparatus configured for "computing a difference frame . . . temporarily buffering the difference frame prior to storing the difference frame in the system memory" and "the apparatus configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Yan, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in claim 18, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 18 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So, in View of U.S. Patent No. 4,546,383 to Abramatic and further in view of U.S. Patent No. 5,926,223 to Hardiman.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) in view of Abramatic (U.S. Patent No. 4,546,383) and further in view of Hardiman (U.S. Patent No. 5, 926, 223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 19 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

(5) Regarding claim 19, Dea, So, Abramatic, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claim in claim 19, including all of the claim limitations of the base claim, namely, an apparatus configured for "computing a difference frame . . . temporarily buffering the difference frame prior to storing the difference frame in the system memory" and "the apparatus configured to operate within a north bridge chip of the computer system **to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit**". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 19, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 19 be withdrawn.

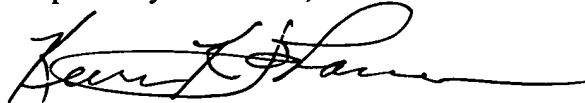
ENTRY OF AMENDMENTS

The amendments to claims 1-5, 13-16 and 20 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-16 and 18-20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,



Kevin K. Johanson
Registration Number 38,506
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

KKJ:ah

Date: February 18, 2003

Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Four-times Amended) An apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising:
 - a video input port, for receiving video data for a current video frame;
 - a video input buffer coupled to the video input port, for storing video data from the video input port;
 - a previous frame buffer, for storing at least a portion of a previous video frame;
 - an operation unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from ~~performing an operation between~~ data from the video input buffer and data from the previous frame buffer; and
 - a result buffer coupled to the operation unit, for temporarily buffering ~~storing~~ the difference frame prior to storing the difference frame in the system memory, ~~result of an operation from the operation unit; wherein~~ the apparatus configured to operate within ~~resides inside of~~ a north bridge chip of the ~~for a computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit so that the signals are provided with a higher bandwidth pathway to improve throughput.~~
2. (Amended) The apparatus of claim 1, including a memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a the system memory that stores video data from the video input port and result data from the result buffer.

3. (Amended) The apparatus of claim 2, ~~including a~~ wherein the system memory ~~coupled couples~~ to the memory port for storing the video data from the video input port and ~~result data~~ the difference frame from the result buffer, wherein the video data is stored to in a current frame area in the system memory and the ~~result data~~ the difference frame is stored in a difference frame area in the memory.

4. (Amended) The apparatus of claim 3, wherein the memory stores a current video frame and a previous video frame in the same location in the system memory, allowing the current video frame to be written over the previous video frame.

5. (Amended) The apparatus of claim 3, wherein the system memory also stores instructions and data for a the central processing unit of a the computer system.

6. (Unchanged) The apparatus of claim 1, wherein the operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer.

7. (Unchanged) The apparatus of claim 1, wherein:
the video input buffer stores a block of data from the video input port;
the previous frame buffer stores a block of data from the previous video frame;
the result buffer stores a block of data from the operation unit; and
the operation unit performs an operation between a block of data from the video input port and a block of data from the previous frame buffer.

Claim 8 was previously cancelled

9. (Unchanged) The apparatus of claim 1, wherein the apparatus comprises part of a video conferencing system.

10. (Unchanged) The apparatus of claim 1, including additional resources within the apparatus, from compressing the video data from the video input port.

11. (Unchanged) The apparatus of claim 1, including a color space conversion circuit coupled between the video input port and the video input buffer.

12. (Unchanged) The apparatus of claim 1, wherein the video input buffer is a register that stores less than one video frame.

13. (Four-times Amended) An apparatus for compressing video data in a computer system including a central processing unit, comprising:

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing a least a portion of a previous video frame;

an exclusive-OR unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from ~~performing an exclusive-OR operation between~~ data from the video input buffer and data from the previous frame buffer;

a result buffer coupled to the ~~operation~~ exclusive-OR unit, for temporarily buffering ~~storing the difference frame result of an operation from the operation unit~~;

a memory port coupled to the previous frame buffer and the result buffer, ~~for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer~~; and

a system memory coupled to the memory port for storing the video data from the video

input port and ~~result data~~ the difference frame from the result buffer, wherein the video data is stored to in a current frame in the memory, ~~and the result data is stored in a difference frame in the memory wherein the apparatus configured to operate within resides inside of a north bridge chip of the for a computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit so that the signals are provided with a higher bandwidth pathway to improve throughput.~~

14. (Amended) The apparatus of claim 13, wherein the system memory stores a current video frame and a previous video frame in the same location, allowing the current video frame to be written over the previous video frame.

15. (Amended) The apparatus of claim 13, wherein the system memory stores instructions and data for a the central processing unit of a the computer system.

16. (Amended) The apparatus of claim 13, wherein:
the video input buffer stores a block of data from the video input port;
the previous frame buffer stores a block of data from the previous video frame;
the result buffer stores a block of data from the ~~operation~~ exclusive-OR unit; and
the exclusive-OR unit performs an exclusive-OR operation between a block of data from the video input port and a block of data from the previous frame buffer.

Claim 17 was previously cancelled

18. (Unchanged) The apparatus of claim 13, wherein the apparatus comprises part of a video conferencing system.

19. (Unchanged) The apparatus of claim 13, including a color space conversion circuit coupled between the video input port and the video input buffer.

20. (Four-times Amended) A computer system including resources for compressing video, comprising:

a central processing unit and system memory for further compressing the video within the computer system;

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing a least a portion of a previous video frame;

an operation unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from ~~performing an operation between~~ data from the video input buffer and data from the previous frame buffer; and

a result buffer coupled to the operation unit, for temporarily buffering storing the difference frame prior to storing the difference frame in the system memory, ~~result of an operation from the operation unit;~~ wherein the video input port, the video input buffer, the previous frame buffer, the operation unit, and the result buffer configured to operate within reside inside of a north bridge chip of the ~~for a computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit so that graphic signals are provided with a higher bandwidth pathway to improve throughput.~~